VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification

Please replace the paragraph beginning on page 3, line 6 with the following paragraphs:

Figure 2A ~~2~~ is a diagram illustrating a computer-aided design (CAD) of buried intersignal capacitance mode compensation (BICMC) on a PCB according to one embodiment of the invention.

Figure 2B is a diagram illustrating a CAD of a first layer of the PCB shown in Figure 2A.

Figure 2C is a diagram illustrating a CAD of a second layer of the PCB shown in Figure 2A.

Please replace the paragraph beginning on page 4, line 11 with the following paragraph:

Figure 1 is a diagram illustrating a parallel plate capacitor 100 in which one embodiment of the invention can be practiced.

Please replace the paragraph beginning on page 5, line 10 with the following paragraph:

Figures 2A-2C are ~~Figure 2 is~~ an illustration of a top view computer-aided design (CAD) layout of the buried intersignal capacitance mode compensation (BICMC) on a printed circuit board ~~broad~~ (PCB) 200 according to one embodiment of the invention.

Please replace the paragraph beginning on page 6, line1 with the following paragraph:

Buried Intersignal Capacitance (BIC) is a method of arranging traces in a PCB that allows the board designer to create a specified amount of capacitance between signals. The BIC is formed by creating parallel plates on adjacent layers of a circuit board while preserving the existing circuit board structure. The BIC is used in mode compensation to

improve signal quality in the PCB. One of the effective placements of the mode compensating capacitor is between adjacent signal traces at the receiver end of the trace. Placing the mode compensation capacitor at the driver end of the two adjacent signal traces is an alternative way to improve signal quality in the PCB. Mode compensation counteracts the tendency of odd-mode crosstalk to travel faster than even-mode crosstalk through a microstrip transmission line. Even-mode crosstalk occurs when a signal line changes its level in one direction and an adjacent signal line changes its level in the same direction (i.e., the signal line is changed from low to high and the adjacent signal line is also changed from low to high). Odd-mode crosstalk occurs when a signal line changes its level in one direction and the adjacent signal line changes its level in the opposite direction (i.e., the signal line is changed from low to high and the adjacent signal line is changed from high to low).

Please replace the paragraph beginning on page 9, line 16 with the following paragraph:

A signal layer 301A includes signal paths 302A and 302B having vias 303A and 303B, respectively. The signal paths 302A and 302B carry signals between devices on the PCB 200. The two signal paths 302A and 302B may be horizontally ~~horizontal~~ adjacent to one another and on the same plane (i.e., signal plane) or may be vertically ~~vertical~~ adjacent to one another on two different but adjacent planes. The via 303A as shown on the signal layer 301A is used to interconnect signal path 302A on the signal layer 301A to the signal path 302A on the next layer 301B. In other words, the signal path 302A extends down from the via 303A to beneath the signal path 302B, turns, and follows parallel to the signal path 302B.

Please replace the paragraph beginning on page 10, line 1 with the following paragraph:

A buried interconnect capacitance (as discussed in reference to Figures 2A-2C) ~~(as discuss in figure 2)~~ is created between the signal path 302B of the signal layer 301A and the

signal path 302A of the next layer 301B. These two paths run immediately above/below each other and are separated by a dielectric layers. The size of the capacitance can be controlled by adjusting the distance between the signal path 302B on signal layer 301A and the signal path 302 on the adjacent routing layer 301B.

In The Claims

1. (Amended) An apparatus comprising:

a first signal path connected to a first plane via a plated hole, the first signal path on a second plane;

a first metal flood connected to the plated hole to form a first plate, the first metal flood on the first plane;

a second signal path on ~~a~~ the second plane; and

a second metal flood connected to the second signal path to form a second plate above the first plate, the second plate on the second plane.

8. (Amended) A method comprising:

connecting a first signal path to a first plane via a plated hole, the first signal path on a second plane;

forming a first plate by connecting a first metal flood to the plated hole, the first metal flood on the first plane; and

connecting a second metal flood to a second signal path on the second plane to form a second plate above the first plate.

15. (Amended) A system comprising:

a through hole component to hold a component that is mounted on a board, the through hole component having one of a first receiver end and a first driver end; a signal carrying module coupled to the through hole component to carry signal, the signal carrying module comprising:

a first signal path connected to a first plane via a plated hole, the first signal path on a second plane;

a first metal flood connected to the plated hole to form a first plate, the first metal flood on the first plane;

a second signal path on ~~a~~ the second plane; and

a second metal flood connected to the second signal path to form a second plate above the first plate, the second plate on the second plane.

22. (New) The apparatus of claim 1 further comprising:

a dielectric layer between the first plate and the second plate.

23. (New) The apparatus of claim 2 wherein the capacitance is a buried intersignal capacitance.

24. (New) The method of claim 8 further comprising:

forming a dielectric layer between the first plate and the second plate.

25. (New) The method of claim 9 wherein the capacitance is a buried intersignal capacitance.

26. (New) The system of claim 15 further comprising:

forming a dielectric layer between the first plate and the second plate.

27. (New) The system of claim 16 wherein the capacitance is a buried intersignal capacitance.

28. (New) An apparatus comprising:

a printed circuit board;

a first transmission line on a first layer of the printed circuit board;

a second transmission line on the first layer of the printed circuit board; and

a capacitor connected to the first transmission line and the second transmission line, the capacitor comprising:

a first plate connected to the first transmission line by a plated hole, the first plate on a second layer of the printed circuit board;

a second plate connected to the second transmission line, the second plate on the first layer of the printed circuit board; and

a dielectric layer between the first plate and the second plate, the dielectric layer between the first layer of the printed circuit board and the second layer of the printed circuit board.

29. (New) The apparatus of claim 28 wherein the first plate is above the second plate.

30. (New) The apparatus of claim 28 wherein the second plate is above the first plate.

31. (New) The apparatus of claim 28 wherein the capacitor is a buried intersignal capacitor.

32. (New) The apparatus of claim 31 wherein the buried intersignal capacitor mode compensates to improve signal quality in the printed circuit board.

33. (New) The apparatus of claim 32 wherein the buried intersignal capacitor matches the propagation speed of odd-mode switch signals with the propagation speed of even-mode switch signals.

34. (New) The apparatus of claim 28 wherein the first layer of the printed circuit board and the second layer of the printed circuit board are adjacent layers.

35. (New) The apparatus of claim 28 wherein the first plate is connected at a first receiver end of the first transmission line and the second plate is connected a second receiver end of the second transmission line.

36. (New) The apparatus of claim 28 wherein the first plate is connected at a first driver end of the first transmission line and the second plate is connected at a second driver end of the second transmission end.

37. (New) The apparatus of claim 28 wherein the first transmission line is adjacent to the second transmission line.

38. (New) The apparatus of claim 28 wherein the first transmission line is inductively coupled to the second transmission line.

39. (New) The apparatus of claim 28 wherein the first transmission line and/or second transmission line are routed as microstrips.

40. (New) The apparatus of claim 28 wherein first transmission line and the second transmission line are routed on surface layers of the printed circuit board.